Customer No.:31561
Application No.: 10/711,939
Docket No.: 11438-US-PA-0P

REMARKS

Present Status of the Application

This application is a CIP of 10/605,199 filed on September 15, 2003 which is a CIP of 10/210,031 filed on August 2, 2002 (Patent No. 6,875,653.

Claims 1-22 are pending.

The Office Action rejected claims 1, 2, 5, 6, 11, 15 and 16 under 35 U.S.C. 102(b) as being anticipated by Schrems US 6,608,341.

Applicant notes that the Examiner has kindly pointed out the allowability of claims 3, 4, 7-10, 12-14 and 17-22, for which courtesy the Examiner is thanked.

Applicant submits that a typing error occurred in the specification has been corrected as instructed by the Examiner. No other amendment has been made and no new matter is entered hereby.

Claim Rejections Under 35 U.S.C. §102

The Office Action rejected claims 1, 2, 5, 6, 11, 15 and 16 under 35 U.S.C. 102(b) as being anticipated by Schrems US 6,608,341. Responsive to the rejections, Applicant hereby otherwise respectfully traverses the rejections. As such, Applicant submits that claims 1, 2, 5, 6, 11, 15 and 16 are now in condition for allowance.

With respect to claim 1, as originally filed, recites in parts:
A dynamic random access memory (DRAM) cell, comprising:
a semiconductor pillar on a substrate;

a capacitor on a lower portion of a sidewall of the pillar, comprising:

...

a third plate at periphery of the second plate, **electrically connecting with the first plate to form a lower electrode together**; and
a dielectric layer, separating the second plate from the first plate and the third plate ... (Emphasis added)

Applicant submits that such a DRAM cell, as originally filed is neither taught, suggested, nor disclosed by Schrems, or any of the other cited references, taken alone or in combination.

First of all, Schrems fails to teach, suggest or disclose "a semiconductor pillar on a substrate". Schrems teaches "[T]he memory cell 100 illustrated includes **a trench capacitor** 160 and a transistor 111", "[T]he trench capacitor 160 is **formed in a substrate** 101" (Column 6, lines 10-12; FIG. 1; Emphasis added), and "[T]he trench 108 is filled with **a conductive trench filling** 161" (Column 6, lines 33, 34; Emphasis added). Applicant submits that, at least to those of ordinary skill in the art, a **trench** capacitor formed **in** a substrate as set forth in Schrems does not read on a **pillar on** a substrate as set forth in claim 1, and a trench formed by filling of a **conductive trench** filling does not read on a **semiconductor pillar** as set forth in claim 1 (Emphasis added).

Second, Schrems fails to teach, suggest or disclose "a third plate ... electrically connecting with the first plate to form a lower electrode together" as set forth in claim 1. The Examiner contends that items pate161 and 165 of Schrems respectively read on the third plate and the first plate. However, as shown in FIG. 1 of Schrems, item 165 is a buried plate "provided around the lower region 110" and configured at a peripheral of the conductive layer

310 that is alleged as reading on the second plate as set forth in claim 1, while item 161 is a trench filling "which forms the inner capacitor electrode" that is isolated from the conductive layer 310 by a "dielectric layer 164 which forms the storage dielectric" (Column 6, lines 19-34). According to Schrems, items 161 and 165 are electrically isolated or insulated from each other, rather than electrically connected, thus they have no way to form an electrode together.

Third, Schrems fails to teach, suggest or disclose "**a dielectric layer, separating the second plate from the first plate and the third plate** ..." (Emphasis added). As shown in FIG. 1 of Schrems, item 310 and 165 are not separated from each other at all, thus they are not separated by item 168. Item 310 and item 161 are separated from each other, however what separates them from each other is item 164 rather than item 168.

Accordingly, Schrems fails to teach each and every element as set forth in claim 1, either expressly or inherently, and thus claim 1 and its dependent claims 2, 5 and 6 are submitted to be novel and unobvious over Schrems and should be allowed.

With respect to claim 11, as originally filed, recites in parts:

A ... (DRAM) array, comprising:

...

cells ..., each comprising:

a semiconductor pillar on the substrate;

a capacitor ... comprising a first plate ..., a second plate ..., a third plate ... **electrically connected with the first plate to form a lower electrode together, and a dielectric layer separating the second plate from the first plate and the third plate**

... (Emphasis added)

Applicant submits that such a DRAM cell, as originally filed is neither taught, suggested, nor disclosed by Schrems, or any of the other cited references, taken alone or in combination.

Similar to the foregoing reasons addressing to claim 1 discussed above, Schrems fails to teach, disclose or suggest "a **semiconductor pillar on a substrate**", "a **third plate ... electrically connected with the first plate to form a lower electrode together**", and "a **dielectric layer, separating the second plate from the first plate and the third plate ...**" (Emphasis added).

Accordingly, Schrems fails to teach each and every element as set forth in claim 11, either expressly or inherently, and thus claim 11 and its dependent claims 15 and 16 are submitted to be novel and unobvious over Schrems and should be allowed.

Allowable Subject Matter

The Examiner objects claims 3, 4, 7-10, 12-14 and 17-22 as being dependent upon a rejected base claim, and contends that they would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response to the objections, Applicant submits that claims 1 and 11 are allowable as discussed above, upon which claims 3, 4, 7-10, 12-14 and 17-22, which remain unchanged, respectively depend. Therefore, claims 3, 4, 7-10, 12-14 and 17-22 are also allowable.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-22 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : May 16, 2006

Respectfully submitted,

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